AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below. A complete listing of all pending claims is presented.

1. (Currently-Amended) A sine wave generation circuit for stepwisely changing a voltage level of an output signal in synchronization with an input clock signal [to generate] and generating a pseudo sine wave, comprising:

a pulse generation circuit for generating a plurality of pulse signals [using] in synchronization with said clock signal[as a reference]; and

a voltage output circuit having a plurality of coefficient generation circuits, for generating a voltage signal proportional to a plurality of different coefficients generated in said coefficient generation circuits in response to [the combination of bit information in] said plurality of pulse signals and stepwisely changing the voltage level of said output signal, [in response to a coefficient series obtained when further combining the generated plurality of coefficients,]

said plurality of coefficient generation circuits generating said plurality [provided in said voltage output circuit and generating said plurality] of coefficients [including] of an odd number [generation circuits for generating odd number values of] at least ternary-coefficient-values [inculuding] including a first coefficient[s], and, a second coefficient at [on] a positive side and a third coefficient[s] [on] at a negative side arranged symmetrically about a center of the first coefficient.

2. (Currently-Amended) A sine wave generation circuit as set forth in claim 1, wherein when the number of [the] said plurality of coefficient generation circuits is n, where [()]n is a

natural number equal or greater than of 2, [or more),] said n number of coefficient circuits includes, at least (n-1) [n] number of ternary-value generation circuits[are included in the n number of coefficient generation circuits].

3. (Currently-Amended) A sine wave generation circuit as set forth in claim 2, wherein said plurality of coefficient generation circuits comprise a voltage generation circuit, said voltage generation circuit includes:

one binary-value generation circuit for alternately outputting a positive coefficient value and a negative coefficient value [under] in accordance with the control of said pulse signals; and

the (n-1) number of ternary-coefficient-value generation circuits for repeatedly outputting a reference value, and a coefficient value[s] at the positive side and another coefficient value[s] at the negative side [from] to the reference value [under] in accordance with the control of said pulse signals, and

where the voltage generation circuit generates a voltage signal proportional to a odd number sampling value of the sine wave, when carrying out the sampling of the sine wave to perform an equal period sampling of 4xn points including the maximum value and minimum value of the sine wave, and defining the maximum value sampling point as a 0-th number sampling point, and the minimum value sampling point after a half period as 2n-th number sampling point.

[wherein bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n number of equidistant points not including the maximum value, minimum value, and center point between them in a half cycle

period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.]

4. (Currently-Amended) A sine wave generation circuit as set forth in claim 1, wherein:

each of said plurality of coefficient generation circuits [have] has a voltage generation circuit including n number of ternary-value generation circuits repeatedly outputting a reference value, [and values] a value at the positive side of the reference value and a [values] value at the negative side [from] of the reference value, under the control of said pulse signals, and

the voltage generation circuit generates a voltage signal proportional to an even number sampling value of the sine wave, when carrying out the sampling of the sine wave to perform an equal period sampling of 4xn points including the maximum value, and minimum value of the sine wave, and defining the maximum value sampling point as a 0-th number sampling point, and the minimum value sampling point after a half period as 2n-th number sampling point.

[bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n number of equidistant points including the maximum value or minimum value and a center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.]

5. (Currently-Amended) A sine wave generation circuit as set forth in claim 2, wherein

each of said plurality of coefficient generation circuits has a voltage generation circuit including [have] n number of ternary-value generation circuits repeatedly outputting a reference

value, [and] a [values] value at the positive side of the reference value and a [values] value at the negative side [from] of the reference value, under the control of said pulse signals, and

the voltage generation circuit generates a voltage signal proportional to an even number sampling value of the sine wave, when carrying out the sampling of the sine wave to perform an equal period sampling of 4(n+1) points including the maximum value, and minimum value of the sine wave, and defining the maximum value sampling point as a 0-th number sampling point, and the minimum value sampling point after a half period as 2n-th number sampling point.

[bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n+1 number of equidistant points including the maximum value, minimum value, and center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.]

6. (Currently-Amended) A sine wave generation circuit as set forth in claim 1, wherein said plurality of coefficient generation circuits comprise a voltage generation circuit,

said voltage generation circuit includes:

one binary-value generation circuit for alternately outputting a positive value and a negative value under the control of said pulse signals; and

(n-1) number of ternary-value generation circuits for repeatedly outputting a reference value, [and values] a value at the positive side of the reference value and a [values] value at the negative side [from] of the reference value, under the control of said pulse signals, and

the voltage generation circuit generates a voltage signal proportional to an even number sampling value of the sine wave, when carrying out the sampling of the sine wave to perform an equal period sampling of 4(n+1) points including the maximum value, and minimum value of the sine wave, and defining the maximum value sampling point as a 0-th number sampling point, and the minimum value sampling point after a half period as 2n-th number sampling point.

[wherein bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n-1 number of equidistant points including one of the maximum value and minimum value and not including the center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.]

7. (Currently-Amended) A sine wave generation circuit as set forth in claim 1, wherein said pulse generation circuit [is] comprises a shift circuit for [shifting said] outputting a first rectangular signal synchronized with said input clock signal [by exactly a predetermined time, wherein said plurality of coefficient generation circuits comprise:] and a second rectangular signal delayed by a predetermined time width, and

[one binary generation circuit for alternately outputting a positive value and a negative value under the control of said pulse signals; and]

[(n-1) number of] wherein said ternary-value generation circuits add the first rectangular signal and the second rectangular signal to result in an equivalent ternary-value coefficient.[for repeatedly outputting a reference value and values at the positive side and values at the negative

side from the reference value based on a clock signal delayed in phase by exactly said predetermined time from said clock signal generated by said shift circuit and a clock signal advanced in phase by exactly said predetermined time; and

wherein said voltage output circuit generates said pseudo sine wave by adding the binary-value pulse signal output from said binary-value generation circuit and the ternary-value pulse signals output from said ternary-value generation circuits.]